Claims

1. A method to write data to a first memory, comprising:

asserting a write enable signal;

asserting a chip enable signal after the asserting of the write enable signal;

deasserting the chip enable signal to latch the data in the first memory, wherein the deasserting of the chip enable signal occurs after the asserting of the write enable signal; and

deasserting the write enable signal after the deasserting of the chip enable signal.

2. The method of claim 1, further comprising:

sending an address to the first memory, wherein the address is the location in the first memory where the data is to be written; and

latching the address and the data in the first memory on the rising or falling edge of the chip enable signal.

3. The method of claim 1, further comprising:

transmitting the write enable signal to the first memory and to a second memory; and

transmitting the chip enable signal to only the first memory.

4. The method of claim 1, further comprising:

sending the write enable signal to at least two memories; and

sending the chip enable signal to only one memory, wherein the one memory is the first memory.

5. The method of claim 1, wherein the chip enable signal is coupled to a chip enable pin of the first memory, the write enable signal is coupled to a write enable pin of the first memory, the write enable signal is coupled to a write enable pin of a second memory, and the chip enable signal is not coupled to a chip enable pin of the second memory.

6. The method of claim 5, wherein the first memory is a nonvolatile memory and the second memory is a nonvolatile memory .

7. The method of claim 6, wherein the first memory is a flash memory and the second memory is a flash memory.

8. The method of claim 5, wherein the first memory is a volatile memory and the second memory is a nonvolatile memory.

9. The method of claim 8, wherein the first memory is a static random access memory (SRAM) or dynamic random access memory (DRAM) and the second memory is a flash memory.

10. The method of claim 1, further comprising:

using a first multiplexer to generate the chip enable signal; and

using a second multiplexer to generate the write enable signal.

11. The method of claim 1, selecting between two signals to generate the chip enable signal.

12. The method of claim 1, programming a bit to enable either latching of the data in the first memory on the deasserting of the chip enable signal or enable latching of the data in the first memory on the deasserting of the write enable signal.

13. A method to transfer data to one of at least two memories, comprising:

latching the data in a first memory of the at least two memories in response to the rising edge or falling edge of a chip select signal.

14. The method of claim 13, wherein the chip select signal is coupled to the first memory and the chip select signal is only coupled to one memory of the at least two memories.

15. The method of claim 13, wherein the chip select signal is coupled to a chip select pin of the first memory of the at least two memories and is not coupled to a chip select pin of a second memory of the at least two memories.

16. The method of claim 13, further comprising:

asserting a write enable signal that is coupled to a write enable pin of the first memory, wherein the write enable signal is coupled to a write enable pin of a second memory of the at least two memories; and

deasserting the chip select signal to latch the data in the first memory, wherein the deasserting of the chip select signal occurs after the asserting of the write enable signal and prior to deasserting of the write enable signal.

17. The method of claim 16, further comprising:

deasserting an output enable signal while the chip select signal is asserted and the write enable signal is asserted;

transmitting the output enable signal to an output enable pin of the first memory; and

transmitting the output enable signal to an output enable pin of the second memory.

18. The method of claim 16, wherein the first memory is a flash memory and the second memory is a flash memory.

19. The method of claim 16, wherein the first memory is a volatile memory and the second memory is a nonvolatile memory.

20. The method of claim 16, wherein the first memory is stacked on a processor and the first memory is located physically closer to the processor than the second memory.

21. A method to transfer data to one of at least two memories, comprising:

deasserting a chip select signal to latch the data in a first memory of the at least two memories, wherein the deasserting of the chip select signal occurs after asserting of a write enable signal and prior to deasserting of the write enable signal.

22. The method of claim 21, further comprising:

deasserting an output enable signal while the chip select signal is asserted and the write enable signal is asserted;

coupling the output enable signal to an output enable pin of the first memory; and

coupling the output enable signal to an output enable pin of a second memory of the at least two memories.

23. The method of claim 21, further comprising:

coupling the write enable signal to a write enable pin of the first memory;

coupling the write enable signal to a write enable pin of a second memory of the at least two memories; and

coupling the chip select signal to a chip select pin of the first memory, wherein the chip select signal is not coupled to a chip select pin of the second memory.

24. The method of claim 23, wherein the first memory is a flash memory and the second memory is a flash memory.

25. The method of claim 23, wherein the first memory is a volatile memory and the second memory is a nonvolatile memory.

26. The method of claim 23, wherein the first memory is stacked on a processor and the first memory is located physically closer to the processor than the second memory.

27. A memory controller to control the writing of data to a first memory and a second memory, comprising;

a circuit to deassert a chip select signal to latch the data in the first memory after asserting a write enable signal and prior to deasserting the write enable signal, wherein the chip select signal is coupled to the first memory and the write enable signal is coupled to both the first memory and the second memory.

28. The memory controller of claim 27, wherein the chip select signal is not coupled to the second memory.

29. The memory controller of claim 27, wherein the chip select signal is coupled to a chip select pin of the first memory, the write enable signal is coupled to a write enable pin of the first memory, the write enable signal is coupled to a write enable pin of the second memory, and the chip select signal is not coupled to a chip select pin of the second memory.

30. The memory controller of claim 27, wherein the circuit comprises:

a first multiplexer to provide the chip select signal to the first memory; and

a second multiplexer to provide the write enable signal to the first memory and the second memory.

31. The memory controller of claim 27, wherein the first memory is a nonvolatile memory and the second memory is a nonvolatile memory .

32. The memory controller of claim 31, wherein the first memory is a flash memory and the second memory is a flash memory.

33. The memory controller of claim 27, wherein the first memory is a volatile memory and the second memory is a nonvolatile memory.

34. The memory controller of claim 33, wherein the first memory is a static random access memory (SRAM) or dynamic random access memory (DRAM) and the second memory is a flash memory.

35. A system, comprising:

a first memory;

a second memory; and

a processor to deassert a chip select signal to latch the data in the first memory after asserting a write enable signal and prior to deasserting the write enable signal, wherein the chip select signal is coupled to the first memory and the write enable signal is coupled to both the first memory and the second memory; and

an antenna coupled to the processor.

36. The system of claim 35, wherein the chip select signal is coupled to a chip select pin of the first memory, the write enable signal is coupled to a write enable pin of the first memory, the write enable signal is coupled to a write enable pin of the second memory, and the chip select signal is not coupled to a chip select pin of the second memory.

37. The system of claim 35, wherein the first memory is located physically closer to the processor than the second memory.

38. The system of claim 35, wherein the first memory is stacked on the processor and the second memory is not stacked on the processor.

39. The system of claim 35, wherein the first memory is a nonvolatile memory and the second memory is a nonvolatile memory .

40. The system of claim 39, wherein the first memory is a flash memory and the second memory is a flash memory.

41. The system of claim 35, wherein the first memory is a volatile memory and the second memory is a nonvolatile memory.

42. The system of claim 41, wherein the first memory is a static random access memory (SRAM) or dynamic random access memory (DRAM) and the second memory is a flash memory.

43. The system of claim 35, wherein the system is a wireless phone.